Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Cancelled)

3. (Currently Amended) The ~~apparatus~~ switch of claim ~~1~~ 18 wherein the ~~data receive interface~~ fabric interface card comprises:

~~a plurality of data receive devices, each data receive device connected to receive a corresponding sub-stream of data comprising data transmitted by one of the data transmitting devices over the mid-plane via a corresponding one of the first serial connections;~~

a plurality of first direction receive buffers, each first direction receive buffer associated with a corresponding one of the ~~data receive~~ first deserializer devices and configured to receive ~~fixed-length data~~ the first direction packets ~~carried in the corresponding sub-stream~~ from its associated first deserializer device [[; and,]]

~~a first receive control circuit configured to determine a sequence of arrival of the fixed-length data packets at the plurality of buffers~~.

4. (Currently Amended) The ~~apparatus~~ switch of claim 3 wherein the first direction receive control circuit is configured to

provide ~~the~~ first direction receiver enable signals to the first transmit control circuit in response to a status of at least one of the plurality of first direction receive buffers.

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) The apparatus of claim ~~6~~ 11 wherein the ~~first~~ second transmit control circuit is configured to multiplex the flow control signal ~~with the transmit packets in one of the transmit channels~~ into the second data stream.

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) The ~~apparatus~~ switch of claim ~~9~~ 3 wherein the ~~second~~ first direction receive control circuit is configured to issue a first direction flow control signal when any one of the plurality of first direction receive buffers has a remaining capacity of Q packets or fewer, with $Q \geq 1$, wherein the ~~second~~ fabric interface card comprises a transmitter connected to transmit the first direction flow control signal to the line card and wherein the first transmit control circuit is configured, in response to the first direction flow control signal, to inhibit transmission of the ~~transmit~~ first direction packets on at least one of the ***N*** ~~transmit~~ first direction channels corresponding to the

one of the plurality of first direction receive buffers which has the remaining capacity of Q packets or fewer.

11. (Previously Presented) Data transmission apparatus comprising a first transmit interface for transmitting a data stream comprising a sequence of fixed-size transmit packets to a receiver, the first transmit interface comprising:

a first demultiplexer connected to receive the data stream and to split the data stream by delivering the transmit packets in rotation into a plurality of ***N*** transmit channels, so that each said transmit channel carries every N^{th} transmit packet;

a plurality of data transmitting devices, each data transmitting device connected to receive the transmit packets of a corresponding one of the ***N*** transmit channels and to output the transmit packets of the corresponding one of the ***N*** transmit channels on a corresponding data connection for transmitting data over a mid-plane to the receiver, wherein each data transmitting device comprises a serializer device and the corresponding data connection comprises a serial data connection; and,

a first transmit control circuit connected to the data transmitting devices, the first transmit control circuit configured to cause the data transmitting devices to output the transmit packets in sequence with commencement of transmission of the transmit packets from sequential data transmitting devices staggered in time relative to one another by a time difference ΔT;

wherein:

the first transmit interface is located on a line card having an interface for receiving the data stream,

the receiver is located on a second card, and

the serial data connections comprise data lines extending between the line card and the second card through the midplane;

the receiver comprises a second receive interface, the second receive interface comprising:

a plurality of deserializer devices, each of the deserializer devices connected to a corresponding one of the data connections for receiving the transmit packets of the corresponding one of the ***N*** transmit channels after transmission of the transmit packets of the corresponding one of the ***N*** transmit channels from the line card to the second card over the mid-plane;

a plurality of buffers, each of the buffers connected to accept the transmit packets from a corresponding one of the deserializer devices and each of the buffers having a capacity sufficient to hold a plurality of the transmit packets; and,

a second receive control circuit configured to determine a sequence of arrival of the transmit packets in the serial data in the plurality of buffers and to place the transmit packets onto a bus in the sequence of arrival;

wherein:

the second receive control circuit is configured to issue a flow control signal when any one of the buffers has a remaining capacity of Q packets or fewer, with $Q \geq 1$;

the second card comprises a transmitter connected to transmit the flow control signal to the line card; and

the first transmit control circuit is configured, in response to the flow control signal, to inhibit transmission of the transmit packets on at least one of the ***N*** transmit channels corresponding to the one of the buffers which has the remaining capacity of Q packets or fewer; and

the transmitter on the second card comprises a second transmit interface for transmitting a second data stream comprising a second sequence of fixed-size second packets to the line card, the second transmit interface comprising:

a second demultiplexer connected to receive the second data stream and to split the second data stream by delivering the second packets in rotation into a second plurality of ***N*** second channels so that each said second channel carries every ***N***th second packet;

a plurality of second serializer devices, each second serializer device connected to receive the second packets of a corresponding one of the ***N*** second channels and to output the second packets as serial data on one or more second serial data connections over the mid-plane to the line card; and,

a second transmit control circuit connected to the second serializer devices, the second transmit control circuit configured to cause the second serializer devices to output the second

packets of the second data stream in sequence and staggered in time relative to one another by a time difference ΔT.

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (Currently Amended) The ~~data transmission apparatus~~ switch of claim ~~15~~ 18 wherein the first ~~receive interface~~ transmit control circuit is adapted to receive ~~in the data stream~~ a first direction flow control signal originating from the fabric interface card and the first transmit control circuit is ~~connected to receive the flow control signal and~~ adapted to selectively enable or inhibit the transmission of the first direction packets by one of the ~~data transmission~~ first serializer devices in response to the first direction flow control signal.

17. (Currently Amended) The ~~data transmission apparatus~~ switch of claim 16 wherein the ~~first receive interface~~ second direction receive control circuit is adapted to generate a second direction flow control signal and the first transmit control circuit is adapted to cause one of the ~~data transmitting~~ first serializer devices to output the second direction flow control signal.

18. (Previously Presented) A telecommunications switch comprising a plurality of line cards, a switching fabric, a plurality of fabric interface cards connected to the switching fabric and a midplane providing a plurality of data lines connecting the line cards and the fabric interface cards, the telecommunications switch comprising at least one bidirectional interface connecting a line card and a fabric interface card;

the bidirectional interface carrying a first sequence of data packets in a first data stream received at the line card in a first direction from the line card to the fabric interface card and a second sequence of data packets in a second data stream in a second direction from the fabric interface card to the line card;

the bidirectional interface comprising:

a first demultiplexer connected to receive the first data stream and to split the first data stream into a first plurality of ***N*** first direction channels so that each first direction channel carries every ***N***th first direction packet;

for each first direction channel, a first direction serializer device connected to receive the first direction packets of the first direction channel and to output the first direction packets as first direction serial data on one or more first direction serial data connections extending from the line card, through the midplane, to the fabric interface card;

a first transmit control circuit connected to the first direction serializer devices, the first transmit control circuit configured to cause the first direction serializer devices to output the first direction packets in sequence order with commencement of transmission of first direction

packets on different first direction channels staggered in time relative to one another by a time difference ΔT;

a plurality of first deserializer devices at the fabric interface card, the first deserializer devices connected to receive and deserialize the first direction serial data on the first direction serial data connections;

a first direction receive control circuit connected to detect an order of arrival of first direction packets on the first direction serial data connections and to place the first direction packets into a first direction received data stream in the order of arrival of the first direction packets;

a second demultiplexer at the fabric interface card and connected to receive the second data stream and to split the second data stream into a second plurality of N second direction channels so that each second direction channel carries every Nth second direction packet;

for each second direction channel, a second direction serializer device connected to receive the second direction packets of the second direction channel and to output the second direction packets as second direction serial data on one or more second direction serial data connections extending from the fabric interface card, through the midplane, to the line card;

a second transmit control circuit connected to the second direction serializer devices, the second transmit control circuit configured to cause the second direction serializer devices to output the second direction packets in sequence order with commencement of transmission of second direction packets on different second direction channels

staggered in time relative to one another by a time difference ΔT;

a plurality of second deserializer devices at the line card, the second deserializer devices connected to receive and deserialize the second direction serial data on the second direction serial data connections; and,

a second direction receive control circuit connected to detect an order of arrival of second direction packets on the second direction serial data connections and to place the second direction packets into a second direction received data stream in the order of arrival of the second direction packets.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Currently Amended) ~~A method for transmitting a data stream comprising a sequence of fixed-size packets from a transmitter to a receiver, the method comprising:~~ The switch of claim 10, wherein

~~assigning consecutive packets of the data stream into different ones of a plurality of channels;~~

~~simultaneously transmitting data on each of the channels from the transmitter to the receiver while~~

~~staggering commencement of transmission of the cells~~ packets ~~assigned to each channel in time relative to one another by a time difference ΔT;~~

~~inhibiting transmission of packets in at least one of the channels in response to receiving, at the transmitter, a first flow control signal issued from the receiver; and,~~

upon inhibiting transmission of packets in the at least one of the channels, the first transmit control circuit is configured to:

~~waiting~~ wait without transmission of first direction packets in the at least one of the ***N*** first direction channels; and

~~after waiting, recommencing~~ recommence transmission of packets in the at least one of the ***N*** first direction channels an integer multiple of the time difference ΔT after a time at which transmission of a previous packet commenced on the at least one of the ***N*** first direction channels.

25. (Cancelled)

26. (Currently Amended) The ~~method~~ switch of claim ~~20~~ 18 wherein the first ~~sequence of fixed-size packets~~ data stream comprises an OC-192 data stream.

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (Currently Amended) The ~~apparatus~~ switch of claim 3 comprising means for generating a first direction receiver enable signal which causes the first transmit control circuit to disable at least one of the ~~data transmitting~~ first direction serializer devices upon arrival, in one of the plurality of first direction receive buffers, of a second last packet that the one of the plurality of first direction receive buffers can hold.

35. (Currently Amended) The ~~apparatus~~ switch of claim ~~1~~ 18 wherein ~~the sub-streams are staggered in time by a period ΔT, and the period~~ the time difference ΔT is greater than a maximum total skew due to the mid-plane, the ~~data transmitting device~~ the first direction serializer devices and the ~~data receive interface~~ first direction serializer devices.

36. (Cancelled)

37. (Cancelled)

38. (Cancelled)

39. (New) Data transmission apparatus according to claim 11 wherein a rate of data on each of the plurality of ***N*** transmit channels is ***N*** times lower than a data rate of the data stream.

40. (New) The switch of claim 17 wherein the second transmit control circuit is adapted to receive the second direction flow control signal and the second transmit control circuit is adapted to selectively enable or inhibit the transmission of the second direction packets by one of the second serializer devices in response to the second direction flow control signal.